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FUZZY BASED LEAKAGE- AND TEMPERATURE AWARE INSTRUCTION-LEVEL SCHEDULING FOR VLIW

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ABSTRACT

The substantial increase in the leakage component of the total processor energy consumption is due to the miniaturization of devices and the ensuing decrease in the threshold voltage. A large fraction this leakage energy consumption in the functional units is attributed by relatively simpler issue logic and the presence of a large number of function units in the VLIW and the clustered VLIW architectures. However, because of the inherent variations in the ILP of the programs functional units are not fully utilized in the VLIW architectures. Due to the contentions for the limited number of slow inter-cluster communication channels which lead to many short idle cycles, this under utilization is even more pronounced in the context of clustered VLIX architectures. In this paper, we develop a fuzzy based real-time instruction level loop scheduling technique to reduce leakage energy consumption and look up table based temperature-aware workload balance for applications with loops on VLIW architecture. We first prove that the scheduling problem with the minimum leakage energy consumption within a timing constraint is NP-complete. Then, Fuzzy based leakage energy consumption and look up table based temperature-aware workload balance)algorithm is designed to repeatedly regroup a loop based on rotation scheduling , and decrease leakage energy integrating with leakage power reduction mechanism. We conduct experiments on a set of DSP benchmarks based on the power model of the VLIW processors. The results show that our algorithm achieves significant leakage energy saving compared with list scheduling.

Keywords: VLIW architecture, Fuzzy based leakage energy consumption, temperature-aware Scheduling.